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amt

p<sup>+</sup> type semiconductor region (source and drain) 19 with high impurity concentration is, respectively, formed in a memory cell forming region and a peripheral circuit forming region. Although not shown in the figure, a p<sup>+</sup> type semiconductor region 19 is also formed at a part of the p type well 5 in the zener diode forming region (at the lower part of the connection hole 25 shown in FIG. 4) at this time. In addition, arsenic (As) ions and phosphor (P) ions are implanted into the p type well 5, and thereby a n<sup>+</sup> type semiconductor region (source and drain) 20 with high impurity concentration is formed in a peripheral circuit forming region. And, the n<sup>+</sup> type semiconductor region 20 with high impurity concentration is formed in a zener diode forming region. The side wall spacers 18 are formed by performing isotropic etching of a silicon oxide film (not shown) deposited on the substrate 1 by using the CVD method. At this time, dose quantity of boron ion is defined as  $2 \times 10^{15} \text{ cm}^{-2}$  and implantation energy thereof is defined as 10 keV. Dose quantity of arsenic ion is defined as  $3 \times 10^{15} \text{ cm}^{-2}$  and implantation energy thereof is defined as 60 keV. And, dose quantity of phosphor ion is defined as  $5 \times 10^{13} \text{ cm}^{-2}$  and implantation energy thereof is defined as 60 keV.

#### IN THE CLAIMS:

Please **cancel** claims 25 and 28, without prejudice or disclaimer.

Please **amend** claims 1, 3, 22, 24, 26, 27, 29, 32, 36, as follows:

- Sub 1/2  
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1. (**Thrice Amended**) A semiconductor integrated circuit device comprising:  
a semiconductor substrate of a second conductivity type;